Fast Charging Controller IC for multiple USB Interfaces

TypeC/PD2.0/PD3.1, QC5/QC4+/QC3+/QC3.0/QC2.0, FCP, SCP, AFC, SFCP, MTK PE+ 2.0/1.1, UFCS, Apple, BC1.2

1. Features

- **Support Charging standards including**
  - ✧ USB Type-C and USB Power Delivery
    - Support USB PD2.0/PD3.1/PPS
    - Two independent Type-C Source
    - Integrated VCONN power and switch for reading E-Marker cable
  - ✧ Support QC5/QC4+/QC3+/QC3.0/QC2.0
    - Compatible with Class B
  - ✧ Support FCP/SCP
  - ✧ Support AFC
  - ✧ Support SFCP
  - ✧ Support MTK PE+ 2.0/1.1
    - PE+ 2.0: 5~20V (0.5V/step)
    - PE+ 1.1: 5V, 7V, 9V, 12V
  - ✧ Support UFCS
  - ✧ Support BC1.2, Apple 2.4A, SAMSUNG 2.0A
- **Independent built-in shunt regulator**
  - ✧ Programmable constant voltage control
  - ✧ Programmable constant current control
  - ✧ Integrated low side current sense amplifier
  - ✧ Cable drop compensation
- **Support multiple modes of voltage control**
  - ✧ Control of PWM controller feedback
  - ✧ Control of optocoupler
  - ✧ Control of I2C
- **Power management**
  - ✧ Integrated four independent NMOS driver and two of the four support VDS detecting
  - ✧ Integrated Bleeder
  - ✧ Support power saving mode
- **Programmable fault protections**
  - ✧ Over Voltage Protection (OVP)
  - ✧ Under Voltage Protection (UVP)
  - ✧ Over Current Protection (OCP)
  - ✧ Over Temperature Protection (OTP)
  - ✧ DP/DM/CC1/CC2 over voltage protection
- **Operating voltage 3V~25V**
- **Package**
  - ✧ QFN32

2. Description

The IP2738 is a highly integrated fast charging controller dedicated for multiple USB interfaces which supports many kinds of charging standards includes Type-C Source, PD2.0/PD3.1/PPS, HVDCP QC5/QC4+/QC3+/QC3.0/QC2.0 (Quick Charge), FCP (Hisilicon® Fast Charge Protocol), SCP (Super Fast Charge), AFC (Samsung® Adaptive Fast Charge), SFCP, MTK PE+ 2.0/1.1 (MediaTek Pump Express Plus 2.0/1.1), UFCS (Universal Fast Charging for Mobile Devices), BC1.2, Apple 2.4A, SAMSUNG 2.0A.

The IP2738 supports automatically detecting the connected device and switching standards type to respond to the fast charging requirements.

3. Applications

- ✧ Multiple USB power output ports for AC adapter, power bank, car charger, etc.
- ✧ Power supply for smart phones, tablets, netbooks, digital cameras, etc.

4. Typical Application Schematic

- **Independent control of PWM controller feedback**

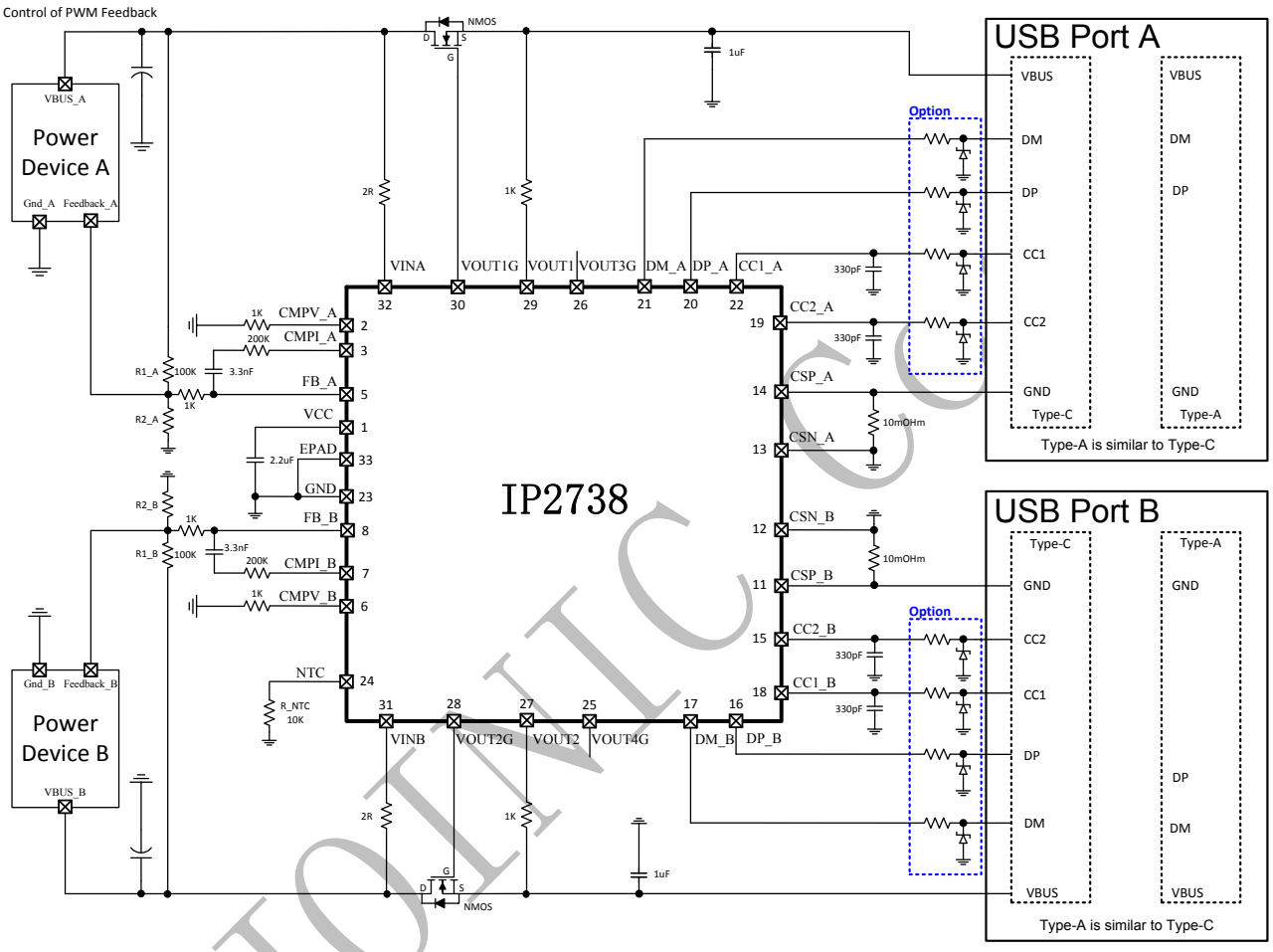


Figure 4-1. Typical application schematic of independent control of PWM controller feedback

Note：

1). 100kOhm(1%) R1_A/R1_B is recommended，R2=(Vfb*R1)/(5-Vfb);

2). Vdss≥30V NMOS is recommended;

3). 10kOhm(B=3380K) R_NTC is recommended;

4). The compensation capacitor and compensation resistor of CMPV/CMPI are adjustable refer to the power device;

- **Independent control of optocoupler**

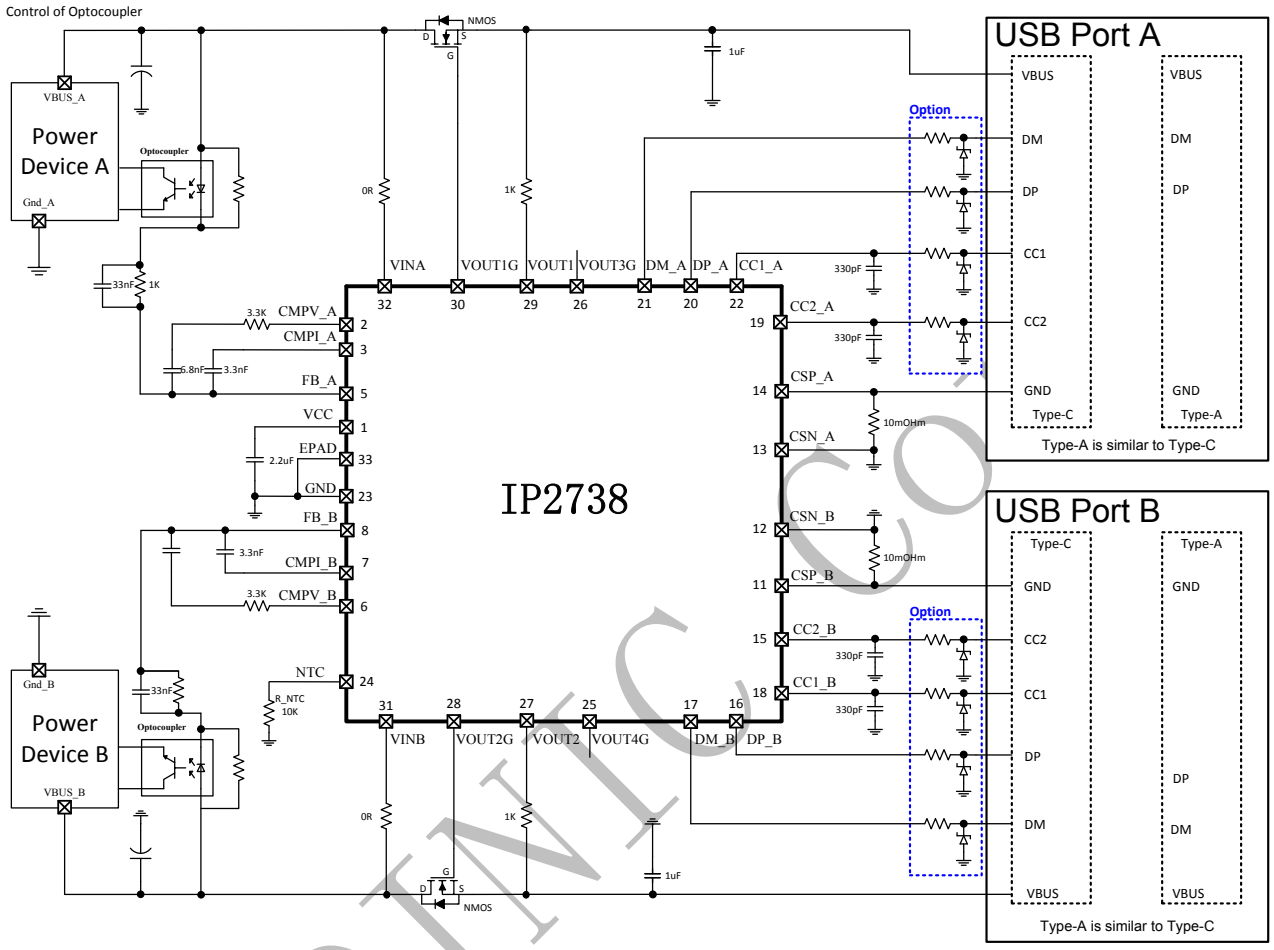


Figure 4-2. Typical application schematic of independent control of optocoupler

Note：

1). Vdss≥30V NMOS is recommended;

2). 10kOhm(B=3380K) R_NTC is recommended;

3). The compensation capacitor and compensation resistor of CMPV/CMPI are adjustable refer to the power device;

- **independent control of I2C**

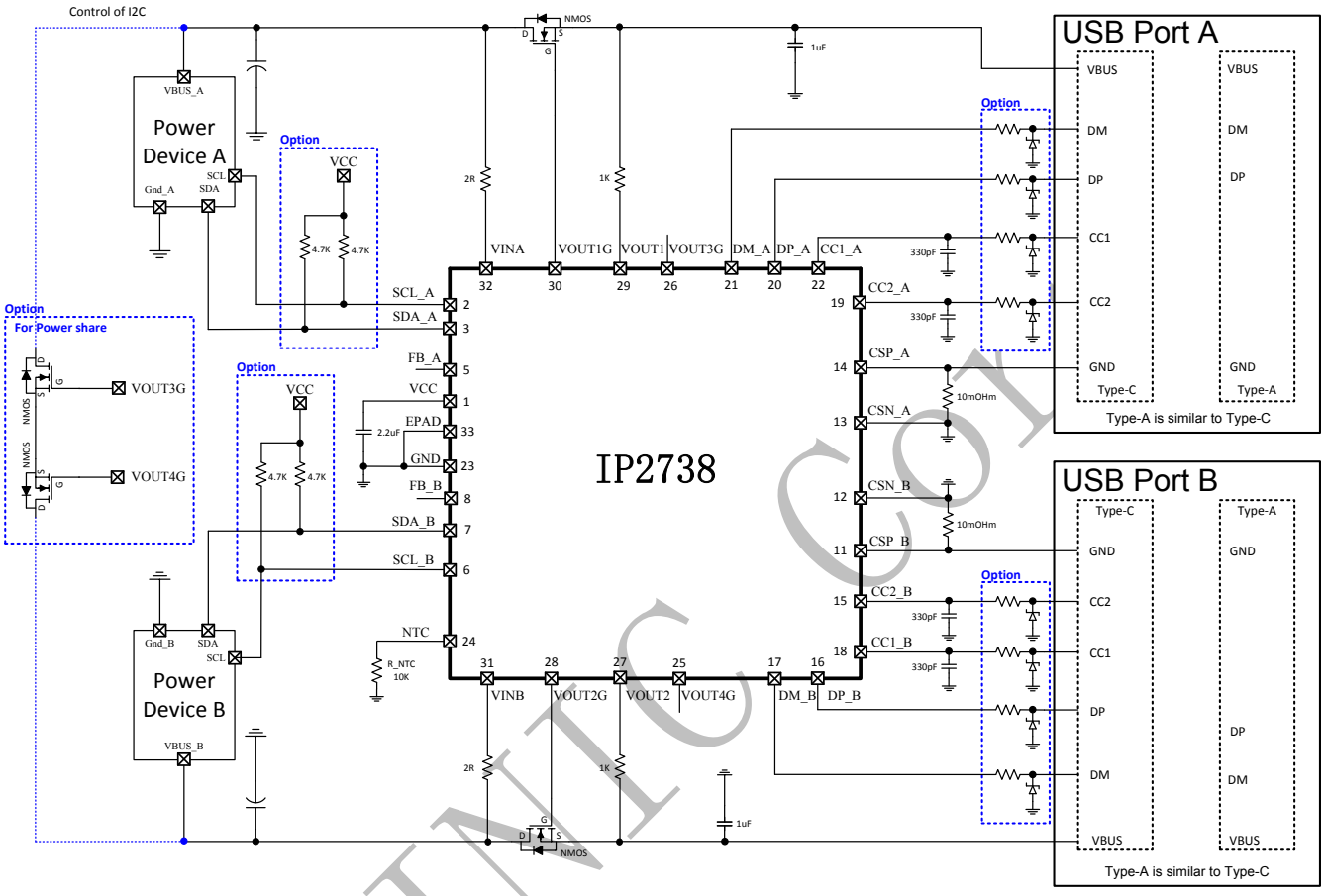


Figure 4-3. Typical application schematic of independent control of I2C

Note：

1). The external pull-up resistor is Optional which can be replace by internal pull-up resistor;

2). Vdss≥30V NMOS is recommended;

3). 10kOhm(B=3380K) R_NTC is recommended;

4). For the power share function, designer should make sure that the Gnd_A of Power Device A and the Gnd_B of Power Device B are independent;

5. Pin Assignment

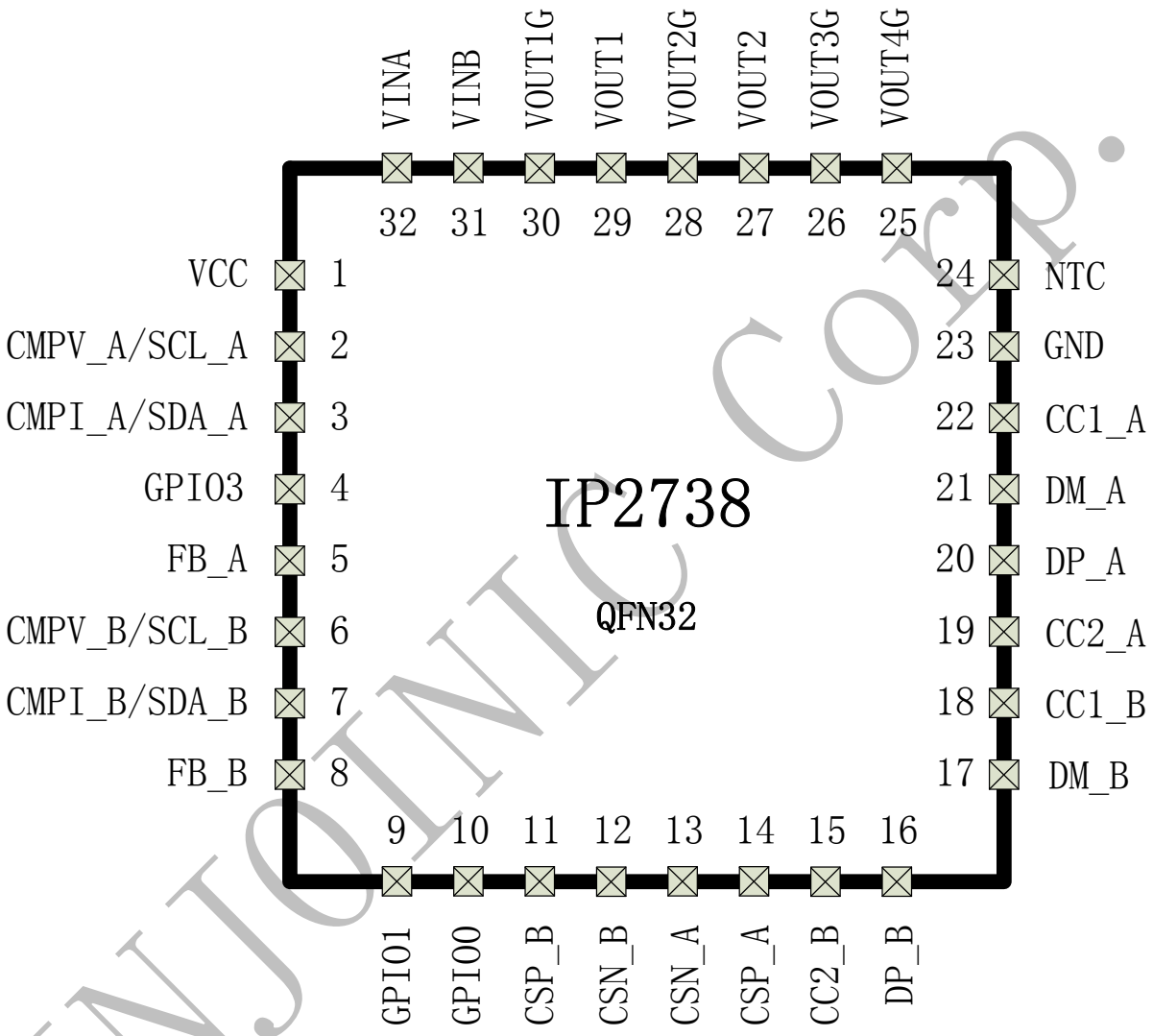


Figure 5-1. Pin Assignment (Top view)

Table 5-1. Pin Description

Pin No.	Pin name	Pin description
1	VCC	Internal power supply output, it is recommended that an external capacitance 2.2uF is used
2	CMPV_A/SCL_A	PortA Loop compensation of voltage / PortA I2C clock
3	CMPI_A/SDA_A	PortA Loop compensation of current / PortA I2C data
4	GPIO3	General purpose I/O 3
5	FB_A	PortA Loop feedback driver
6	CMPV_B/SCL_B	PortB Loop compensation of voltage / PortB I2C clock
7	CMPI_B/SDA_B	PortB Loop compensation of current / PortB I2C data
8	FB_B	PortA Loop feedback driver
9	GPIO1	General purpose I/O 1
10	GPIO0	General purpose I/O 0
11	CSP_B	PortB Positive input of current sense amplifier
12	CSN_B	PortB Negative input of current sense amplifier
13	CSN_A	PortA Negative input of current sense amplifier
14	CSP_A	PortA Positive input of current sense amplifier
15	CC2_B	PortB Type-C Configuration Channel2
16	DP_B	PortB USB DP
17	DM_B	PortB USB DM
18	CC1_B	PortB Type-C Configuration Channel1
19	CC2_A	PortA Type-C Configuration Channel2
20	DP_A	PortA USB DP
21	DM_A	PortA USB DM
22	CC1_A	PortA Type-C Configuration Channel1
23	GND	Ground
24	NTC	NTC Resistor input for temperature sense, built-in current source
25	VOUT4G	PortB Gate driver of load switch 4 (NMOS)
26	VOUT3G	PortA Gate driver of load switch 3 (NMOS)
27	VOUT2	PortB Path detect of load switch 2
28	VOUT2G	PortB Gate driver of load switch 2 (NMOS)
29	VOUT1	PortA Path detect of load switch 1
30	VOUT1G	PortA Gate driver of load switch 1 (NMOS)
31	VINB	PortB Positive power supply
32	VINA	PortA Positive power supply
33	EPAD	Connect to ground

6. Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
VINA, VINB Input Voltage Range	VINA, VINB	-0.3 ~ 30	V
VOUT1, VOUT2 Input Voltage Range	VOUT1, VOUT2	-0.3 ~ 30	V
VOUT1G, VOUT2G Input Voltage Range	VOUT1G, VOUT2G	-0.3 ~ 30	V
VOUT3G, VOUT4G Input Voltage Range	VOUT3G, VOUT4G	-0.3 ~ 30	V
DP_A, DM_A Input Voltage Range	V_{DP_A}, V_{DM_A}	-0.3 ~ 30	V
DP_B, DM_B Input Voltage Range	V_{DP_B}, V_{DM_B}	-0.3 ~ 30	V
CC1_A, CC2_A Input Voltage Range	V_{CC1_A}, V_{CC2_A}	-0.3 ~ 30	V
CC1_B, CC2_B Input Voltage Range	V_{CC1_B}, V_{CC2_B}	-0.3 ~ 30	V
FB_A, FB_B Input Voltage Range	V_{FB_A}, V_{FB_B}	-0.3 ~ 30	V
Other Pins Input Voltage Range		-0.3 ~ 6	V
Junction Temperature Range	T_J	-40 ~ 150	℃
Storage Temperature Range	Tstg	-60 ~ 150	℃
Lead Temperature Range (Soldering, 10sec)	Ts	260	℃
Ambient Temperature	T_A	-40~120	℃
Package Thermal Resistance	θ_{JA}	90	℃/W
Package Thermal Resistance	θ_{JC}	39	℃/W
Human Body Model (HBM)	ESD	4	KV

* Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.

* Voltages are referenced to GND unless otherwise noted.

7. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage	VINA, VINB	3		25	V
Ambient Temperature	T_A	-20		115	℃

* Devices' performance cannot be guaranteed when working beyond those Recommended Operating Conditions.

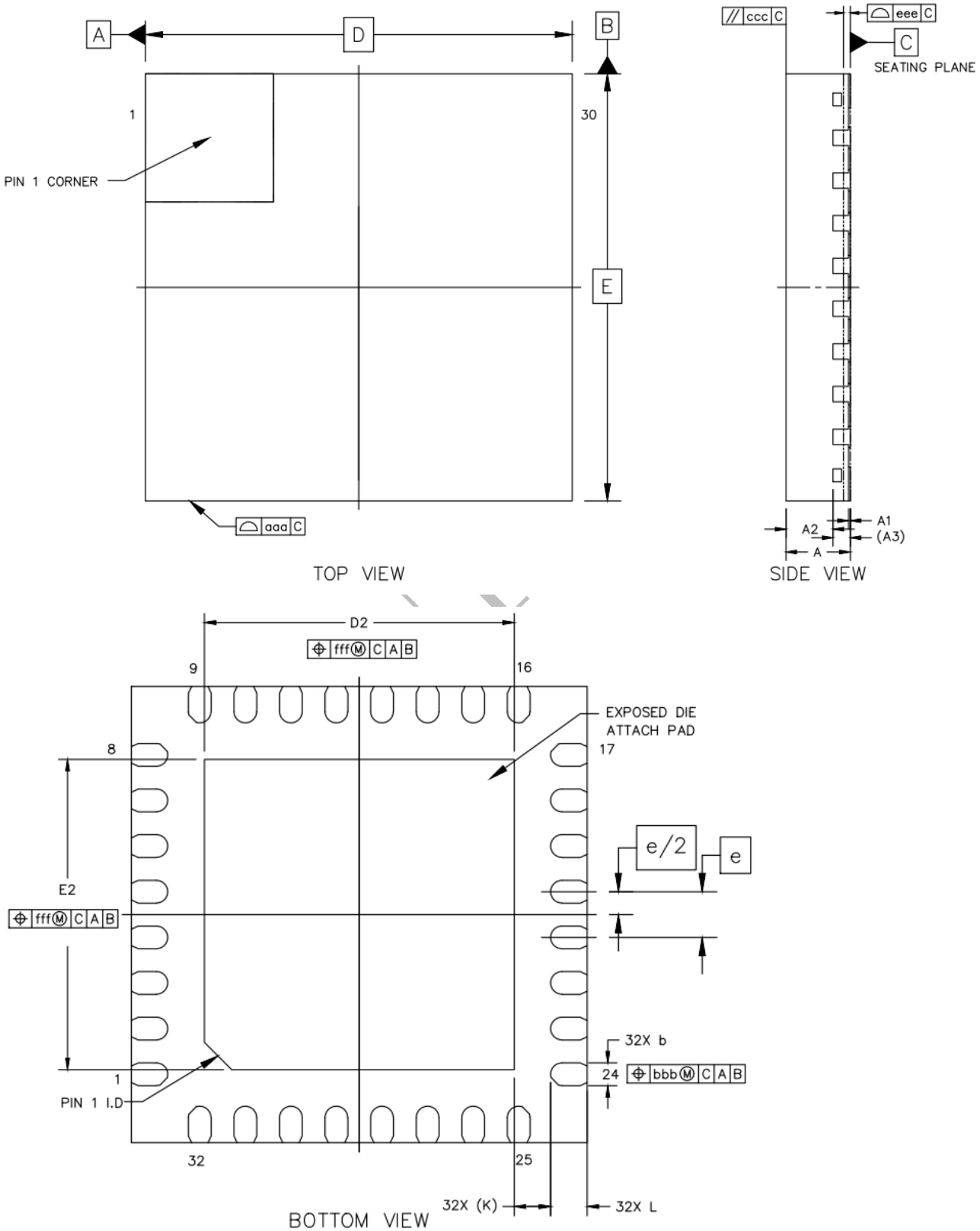
8. Electrical Characteristics

Unless otherwise specified, T A =25℃

Parameter	Symbol	Test Conditions	Min.	Typ.	Max	Unit
Input Voltage	VINA, VINB	Supplied directly	3		25	V
Input UVLO Threshold	UVLO	VINA/VINB Falling	2.5		2.9	V
VCC	VCC			3.2		V
TYPE-C						
Rp_default	Default USB			80		μA
Rp_1.5A	1.5 A @ 5 V			180		μA
Rp_3.0A	3.0 A @ 5 V			330		μA
HVDCP (QC2.0&QC3.0&QC3+)						
Data Detect Voltage Threshold	V_{DATA_REF}		0.25	0.325	0.4	V
DP High Glitch Filter Time	$T_{GLITCH(BC)\_DP\_H}$		1000	1250	1500	ms
DM Low Glitch Filter Time	$T_{GLITCH(BC)\_DM\_L}$			2		ms
Output Voltage Glitch Filter Time	$T_{GLITCH(V)\_CHANGE}$		20	40	60	ms
Continuous Mode Glitch Filter Time	$T_{GLITCH\_CONT\_CHANGE}$		100		200	us
DM Pull-down Resistance	R_{DM_DOWN}	VDP=0.6V		20		kOhm
DP Pull-down Resistance	R_{DAT_LKG}	VDP=0.6V		768		kOhm
DCP						
Samsung DP/DM Output Voltage			1.08	1.2	1.32	V
Samsung DP/DM Output Impedance				100		kOhm
Apple 2.4A DP/DM Output Voltage			2.64	2.7	2.76	V
Apple 2.4A DP/DM Output Impedance				30		kOhm
GPIO						
VIH	Input high voltage		0.7VCC			V
VIL	Input low voltage				0.3VCC	V
VOH	Output high voltage			VCC		V

VOL	Output low voltage			GND		V
Rpu	Pull-up resistor			3		k
Rpd	Pull-down resistor			20		k
I2C						
F_{I2C}	Bit rate		100		400	KHz

9. Package



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	3.3	3.4	3.5
	Y	E2	3.3	3.4	3.5
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.4 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	

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