Fast Charging Physical Layer IC for USB Interfaces

TypeC PD2.0/PD3.0/PPS, QC2.0/QC3.0/QC3+/QC4/QC4+,BC1.2

1. Features

- **Fast charge**
  - ✧ Support QC4/QC4+
    - Compatible with QC2.0/QC3.0
    - Support QC3.0 Class B: 3.6V~20V(0.2V/step)
  - ✧ Support QC3+
    - Support 3.6V~20V(0.02V/step)
    - Support 18W/27W/40W
  - ✧ Support Apple 2.4A, Samsung 2.0A and BC1.2
  - ✧ Support TYPE-C DFP
  - ✧ Support PD2.0/PD3.0/PPS
  - ✧ **USB PD3.0 with PPS Certificate Number：TID:6667**
- **Power Manage**
  - ✧ Build in ADC to monitor the current of the external NMOS FET
  - ✧ Build in power path manage.
  - ✧ Built-in automatic discharge function
  - ✧ Cable drop Compensation
  - ✧ Built-in VCONN power and switch for E-marked cable
- **Power Control Mode**
  - ✧ Optocoupler Mode: Build-in TL431.Drive optocoupler directly
  - ✧ FB Mode: External TL431,connected to feedback node
  - ✧ I2C Mode: Cooperate with the power supply chip, such as Inno3 pro.
- **Multiple protection, high reliability**
  - ✧ Output overcurrent, overvoltage and short circuit protection
  - ✧ NTC over temperature protection
  - ✧ DP,DM,CC1,CC2 overvoltage protection
  - ✧ DP,DM short with GND circuit protection
  - ✧ DP/DM/CC1/CC2 input voltage up to 25V
- **Support 100kHz-400kHz IIC Interface**
- **Working voltage : 3 V~30V**
- **Package : QFN24**

2. Description

IP2732 is a highly-integrated, flexible high voltage charging protocol controller. It supports the most popular high voltage charging protocol, such as TYPE-C, PD2.0/PD3.0, QC2.0/QC3.0, QC3+/QC4/QC4+, BC1.2 etc.

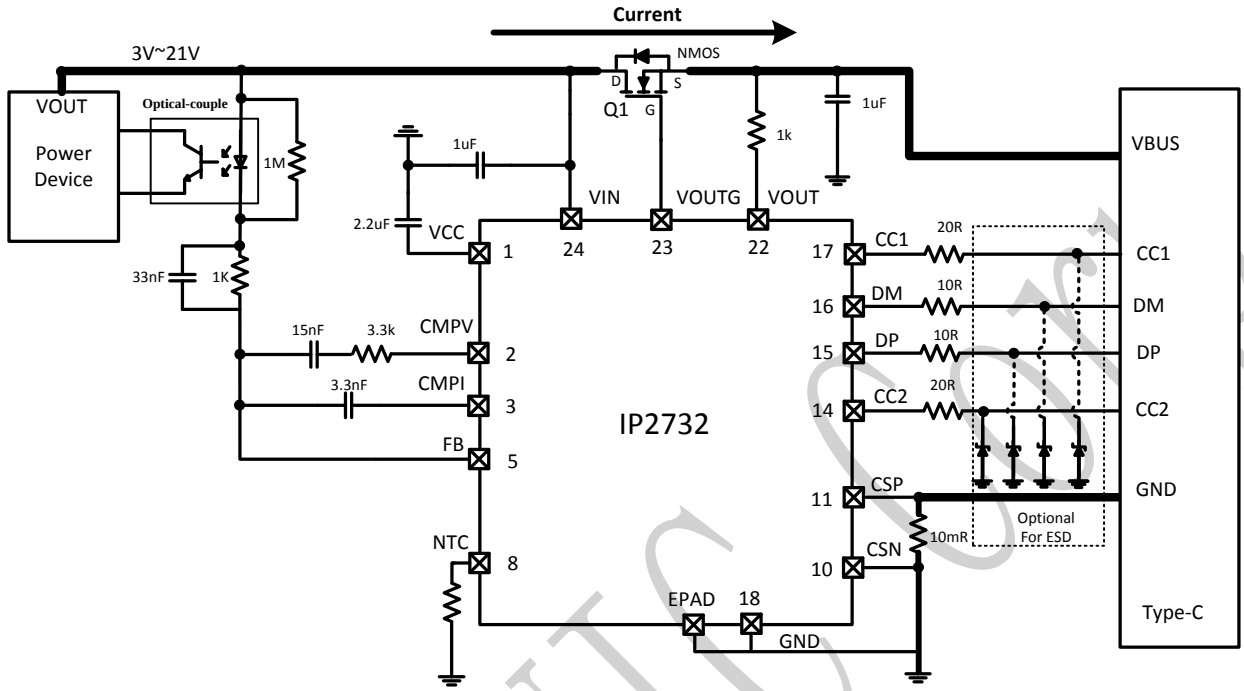
The SOC could be a powerful protocol controller used in AC adapter, power-bank, Car charger or other power charging solution, and make the total solution size minimized and BOM cost down.

3. Typical Applications

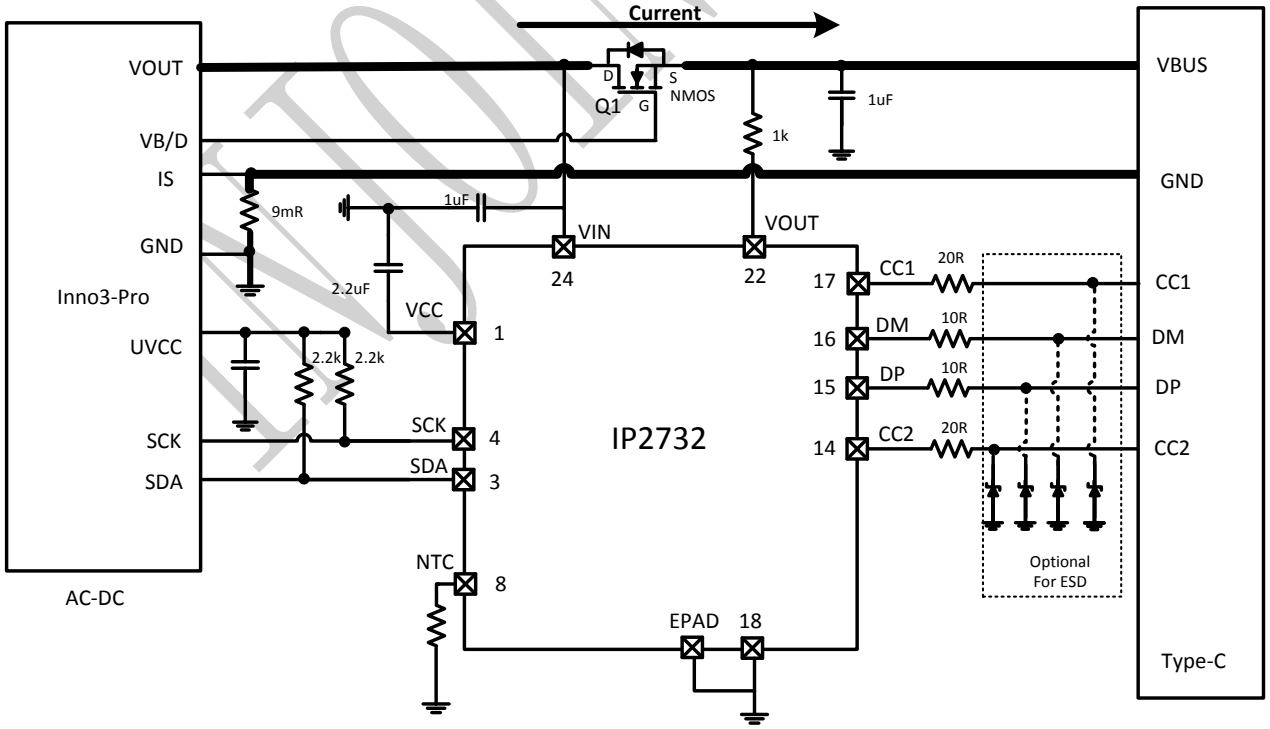
- **USB power output ports for AC adapters, Power Banka, Car chargers**
- **Battery chargers for smart phones, tablets, netbooks, digital cameras, and Bluetooth accessories**

4. Typical Application Schematic

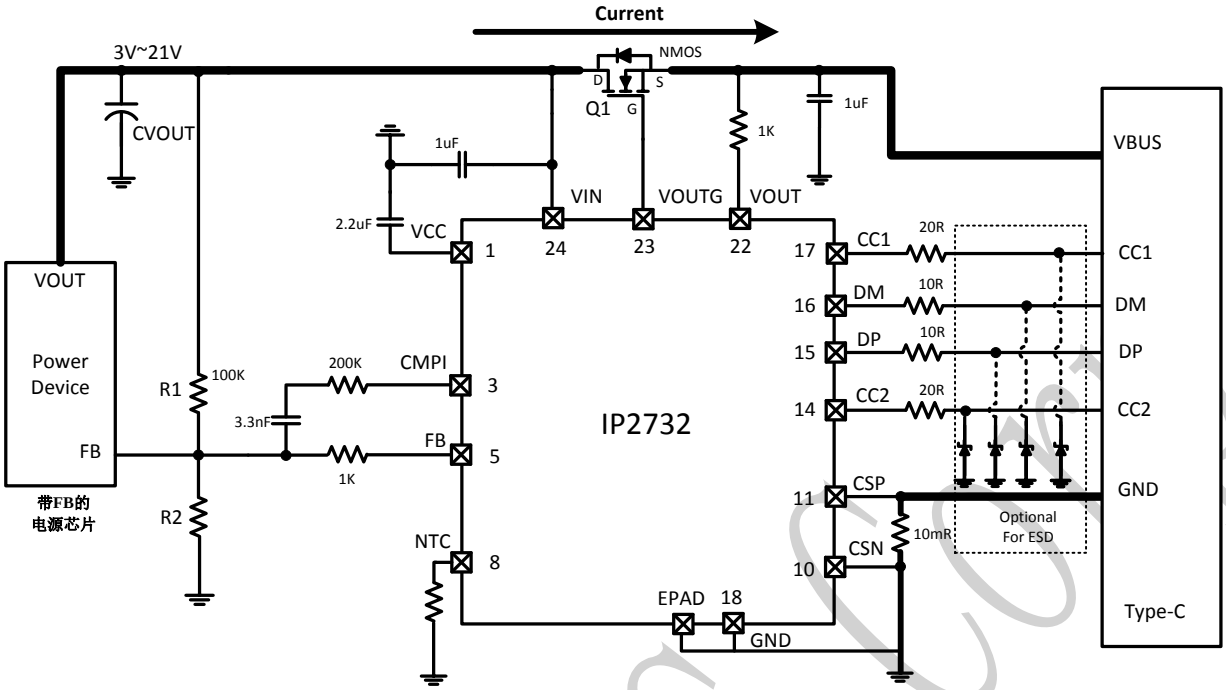
Optocoupler MODE



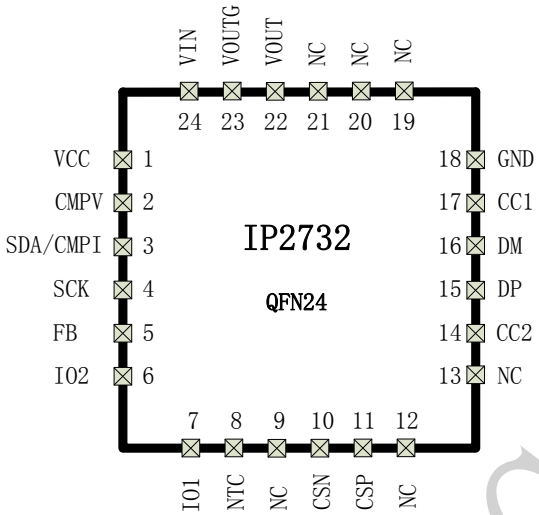
I2C MODE



FB MODE



5. PIN Description



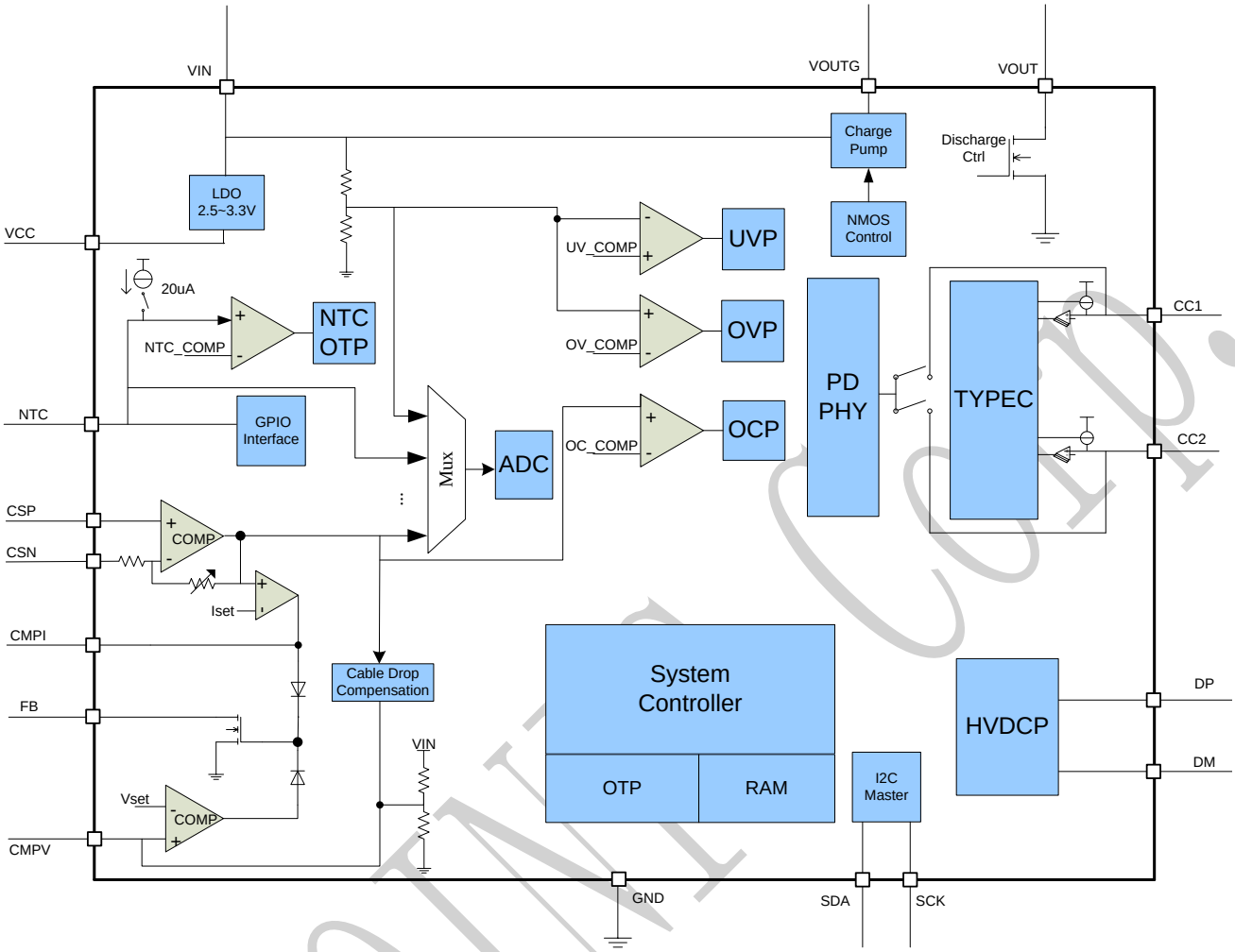
Pin No.	Pin name	Pin description
1	VCC	VCC Internal power supply output, need external 2.2 uF capacitance
2	CMPV	Feedback loop compensation of voltage
3	CMPI/SDA	Feedback loop compensation of current I2C data
4	SCK	I2C clock
5	FB	Feedback PIN. Connect to the FB line of Regulator to the power device with FB control, current source/sink for voltage regulation
6	GPIO2	General purpose IO2
7	GPIO1	General purpose IO1
8	NTC	NTC Resistor input for temperature sense General purpose IO0
9	NC	Not connect
10	CSN	Current sense negative PIN
11	CSP	Current sense positive PIN
12	NC	Not connect
13	NC	Not connect
14	CC2	Type-C CC2 line
15	DP	USB DP data line
16	DM	USB DM data line
17	CC1	Type-C CC1 line
18	GND	ground
19	NC	Not connect
20	NC	Not connect
21	NC	Not connect
22	VOUT	VOUT discharge pin

23	VOUTG	VOUT output path control on the NMOS
24	VIN	Power input

6. Type Specification

型号	模式	PDO/APDO(PPS)配置	QC 配置	QC3+	封装
IP2732_0C20W	光耦	PDO: 5V/3A, 9V/2.22A, 12V/1.67A	ClassA 3.6v-12v	18W	QFN24
IP2732_FB20W	FB				
IP2732_0C20WP	光耦	PDO: 5V/3A, 9V/2.22A, 12V/1.67A PPS: 3.3V-5.9V/3A PPS: 3.3V-11V/1.8A	ClassA 3.6v-12v	18W	QFN24
IP2732_FB20WP	FB				
IP2732_0C25W	光耦	PDO: 5V/3A, 9V/2.77A	ClassA 3.6v-12v	18W	QFN24
IP2732_FB25W	FB				
IP2732_0C25WP	光耦	PDO: 5V/3A, 9V/2.77A PPS: 3.3V-5.9V/3A PPS: 3.3V-11V/2.25A	ClassA 3.6v-12v	18W	QFN24
IP2732_FB25WP	FB				
IP2732_0C30W	光耦	PDO: 5V/3A, 9V/3A, 12V/2.5A, 15V/2A, 20V/1.5A	ClassB 3.6v-20v	27W	QFN24
IP2732_FB30W	FB				
IP2732_0C30WP	光耦	PDO: 5V/3A, 9V/3A, 12V/2.5A, 15V/2A, 20V/1.5A PPS: 3.3V-11V/3A	ClassB 3.6v-20v	27W	QFN24
IP2732_FB30WP	FB				
IP2732_0C45W	光耦	PDO: 5V/3A, 9V/3A, 12V/3A, 15V/3A, 20V/2.25A	ClassB 3.6v-20v	45W	QFN24
IP2732_FB45W	FB				
IP2732_0C45WP	光耦	PDO: 5V/3A, 9V/3A, 12V/3A, 15V/3A, 20V/2.25A PPS: 3.3V-16V/3A	ClassB 3.6v-20v	45W	QFN24
IP2732_FB45WP	FB				
IP2732_0C65W	光耦	PDO: 5V/3A, 9V/3A, 12V/3A, 15V/3A, 20V/3.25A	ClassB 3.6v-20v	45W	QFN24
IP2732_FB65W	FB				
IP2732_0C65WP	光耦	PDO: 5V/3A, 9V/3A, 12V/3A, 15V/3A, 20V/3.25A PPS: 3.3V-21V/3.25A	ClassB 3.6v-20v	45W	QFN24
IP2732_FB65WP	FB				
可定制	可定制	可定制	可定制	可定制	QFN24

7. Internal Block Diagram



8. Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
VIN Input Voltage Range	VIN	-0.3 ~ 30	V
VOUT Input Voltage Range	VOUT	-0.3 ~ 30	V
FB Input Voltage Range	FB	-0.3 ~ 30	V
DP，DM Input Voltage Range	V_{DP}，V_{DM}	-0.3 ~ 25	V
CC1，CC2 Input Voltage Range	V_{CC1}，V_{CC2}	-0.3 ~ 30	V
Other Pins Input Voltage Range		-0.3 ~ 6	V
Junction Temperature Range	T_J	-40 ~ 150	℃
Storage Temperature Range	Tstg	-60 ~ 150	℃
Lead Temperature Range	Ts	260	℃

(Soldering, 10sec)			
Ambient Temperature Range	T_A	-40~120	℃
Package Thermal Resistance	θ_{JA}	90	℃/W
Package Thermal Resistance	θ_{JC}	39	℃/W
Human Body Model (HBM)	ESD	4	KV
Moisture Sensitivity Level (MSL)	MSL	3	Level

* Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.

*Voltages are referenced to GND unless otherwise noted.

9. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Voltage	VIN	3		25	V
Ambient Temperature	T_A	-40		85	℃

* Devices' performance cannot be guaranteed when working beyond those Recommended Operating Conditions.

10.Electrical Characteristics

Unless otherwise specified, TA=25℃, 4.5V ≤ VIN ≤ 5.5V

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Voltage	VIN	Supplied directly	3		25	V
Input UVLO Threshold	UVLO	VIN/VCC Falling	2.5		2.9	V
Output Voltage Range	VOUT		3		21	V
Output Voltage Range Accuracy	△VOUT		-3		3	%
OCP current point	I_{OCP}	Rs=10mR, TA=25℃	0.2		6.4	A
OCP current point accuracy	$\triangle I_{OCP}$	Rs=10mR, TA=25℃	-150		+150	mA
Quiescent Current	I_{NOR}	No load, CC pin connect, VIN=5V	3	4	5	mA
	I_{STDBY}	Standby mode, CC pin floating, VIN=5V	0.4	0.8	1.2	mA
HVDCP (QC2.0&QC3.0)						
Data Detect Voltage Threshold	V_{DATA_REF}		0.25	0.325	0.4	V

Output Voltage Selection Reference	V_{SEL_REF}		1.8	2	2.2	V
DP High Glitch Filter Time	$T_{GLITCH(BC)\_DP\_H}$		1000	1250	1500	ms
DM Low Glitch Filter Time	$T_{GLITCH(BC)\_DM\_L}$		1	2	3	ms
Output Voltage Glitch Filter Time	$T_{GLITCH(V)\_CHANGE}$		20	40	60	ms
Continuous Mode Glitch Filter Time	$T_{GLITCH\_CONT\_CHANGE}$		100		200	us
DM and DP Short Resistance	R_{SHORT}	V_{DP}=0.6V	20	30	40	Ohm
DM Pull-down Resistance	R_{DM_DOWN}	V_{DP}=0.6V	14.25	20	24.8	kOhm
DP Pull-down Resistance	R_{DAT_LKG}	V_{DP}=0.6V	200	500	800	kOhm
DCP						
Samsung DP/DM Output Voltage			1.08	1.2	1.32	V
Samsung DP/DM Output Impedance			70	100	130	kOhm
Apple 2.4A DP/DM Output Voltage			2.64	2.7	2.76	V
Apple 2.4A DP/DM Output Impedance			20	30	40	kOhm
NTC						
NTC OTP Current Source	I_{OTP}		19.4	20	20.6	uA
NTC OTP Voltage Threshold	V_{OTP}		0.1		3	V

11.Function Description

DP/DM Quick Charge

IP2732 can automatically detects Quick Charge 2.0/3.0 /QC3+ capable devices with handshake by USB D+/D- data line. It's also complaint with BC1.2.

- BC1.2: Shorting D+ Line to D- Line.
- QC3+: Support 18W/27W/40W. It can be disabled independently.
- Quick Charge 2.0/3.0: D+ and D- line configuration see **Table 1**.

Table 1 QC2.0/3.0 DP/DM configuration:

DP	DM	Result(Class A)	Result(Class B)
0.6 V	GND	5 V	5 V
3.3 V	0.6 V	9 V	9 V
0.6 V	0.6 V	12 V	12 V
0.6 V	3.3 V	Continue Mode	Continue Mode
3.3 V	3.3 V	Keep	20V

TYPE-C

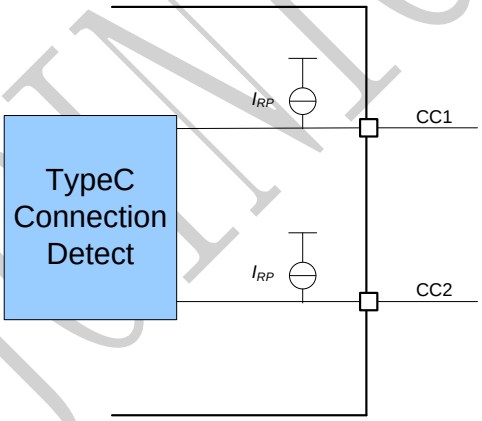
Two pins on the TypeC connector, CC1 and CC2 are used to establish and manage the Source-to-Sink connection.

Only CC1 is used for USB-A connector.

TypeC source exposes independent pull-up(Rp) teminations by current sources on CC1 and CC2 pins to advertise current capability and monitors the voltage by multiple comparators to detect a attach/detach.

The USB Type-C connector uses CC pins for configuration including the ability for a Source to advertise to its port partner (Sink) the amount of current it can apply:

- Default values defined by the USB Specification (500 mA for USB 2.0 ports, 900 mA for USB 3.1 ports)
- 1.5A
- 3.0A



PD Physical Layer

The USB PD Physical Layer consists of a pair of transmitters and receivers that communicate across a single signal wire (CC).

The transmitter performs the following functions:

- Receive packet data from the protocol layer.
- Calculate and append a CRC.

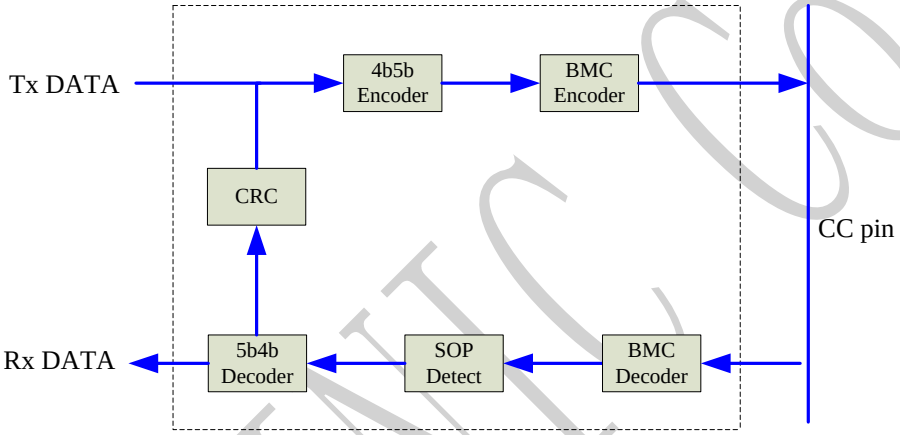
- Encode the packet data including the CRC (i.e. the payload).
- Transmit the Packet (Preamble, SOP*, payload, CRC and EOP) across the channel using Biphase Mark Coding (BMC) over CC.

The receiver performs the following functions:

- Recover the clock and lock onto the Packet from the Preamble.
- Detect the SOP*.
- Decode the received data including the CRC.
- Detect the EOP and validate the CRC:

  If the CRC is Valid, deliver the packet data to the protocol layer.

  If the CRC is Invalid, flush the received data.



VOUT Discharge

When the device is unplugged, the VOUT pin can discharge energy to meet the time requirements of the USB- PD protocol

Voltage regulation mode

➢ FB Mode

IP2732 integrated FB control line used for accurate voltage regulation by source/sink current with precise 2uA/step in minimum. FB sink 40uA current for 9V output voltage; FB sink 70uA current for 12V output voltage; FB sink 150uA current for 20V output voltage; when the output voltage is default 5V, FB neither source nor sink current.

In typical applications, IP2732 FB connects to the regulator's FB line, resistor (R1) between VOUT and FB should apply 100kOhm with high precision (1%), resistor (R2) value between FB and GND should refer to the

regulator adopted, resistance of R2 can be calculated by equation:

$$VFB = \frac{VOUT}{R1 + R2} * R2$$

➢ Optocoupler Mode

IP2732 integrates an optocoupler driver circuit, and the FB pin is connected to the Cathode end of the optocoupler for use in isolated power supplies. The value of external compensation network capacitance, resistance of CMPV and CMPI needs to be adjusted according to the specific parameters of the front-end power network, The CMPV compensation network is used to achieve VOUT output voltage stability. The CMPI compensation network is used to achieve stability of power control.

➢ I2C Mode

IP2732 integrate I2C master control interface, can cooperate with the power supply chip, such as Inno3 pro etc.

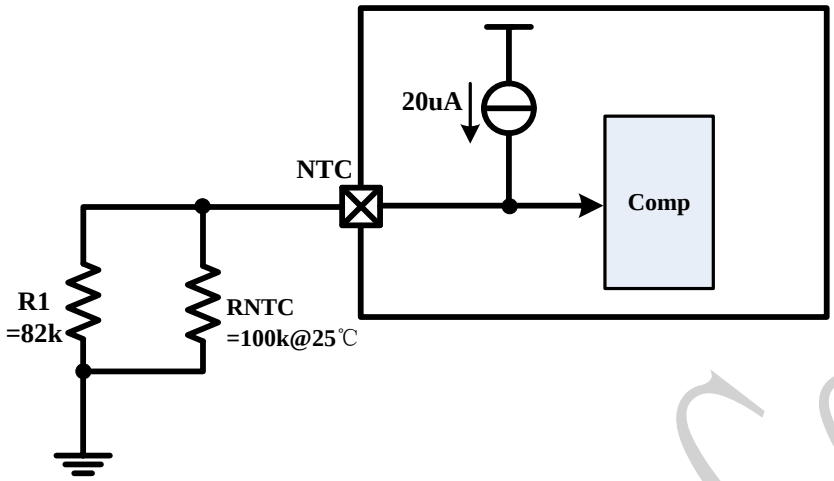
Cable Drop Compensation

IP2732 integrates the line compensation function, which can increase the output voltage in a certain proportion according to the current output current to compensate for linear loss. FB mode and Optocoupler mode can be increased according to the compensation coefficients of 0mV/A, 62.5mV/A, and 125mV/A.

For example, if the compensation coefficient of 125mV/A is selected, if the no-load output voltage is 5.0V, then the actual output voltage=5.0V+3A*125mV/A=5.375V when the output current is 3A

Protections

➢ NTC



IP2732 support NTC function used for temperature detection. NTC pin output 20uA current then detect the voltage on NTC pin to determine the present temperature.

➢ OVP and UVP

IP2732 realizes over-voltage and under-voltage protection functions by detecting the voltage of VIN. The over-voltage threshold and the under-voltage threshold can be flexibly set according to the percentage of the current output voltage. When an abnormal event of over-voltage or under-voltage occurs, the Gate will be pulled low and the external path NMOS transistor will be closed. If the abnormal event disappears, the Type-C handshake and PD communication will be re-established.。

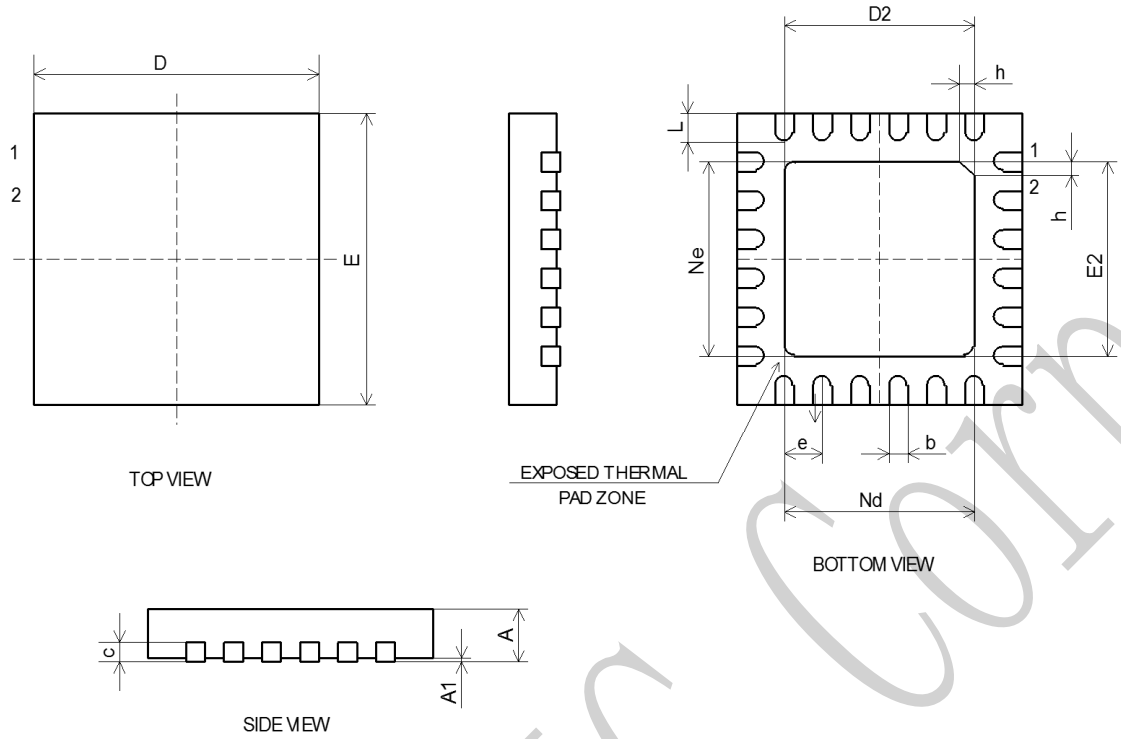
➢ OTP

IP2732 integrates internal junction temperature OTP protection. Junction temperature protection occurs when the junction temperature exceeds 135 ℃

➢ OCP

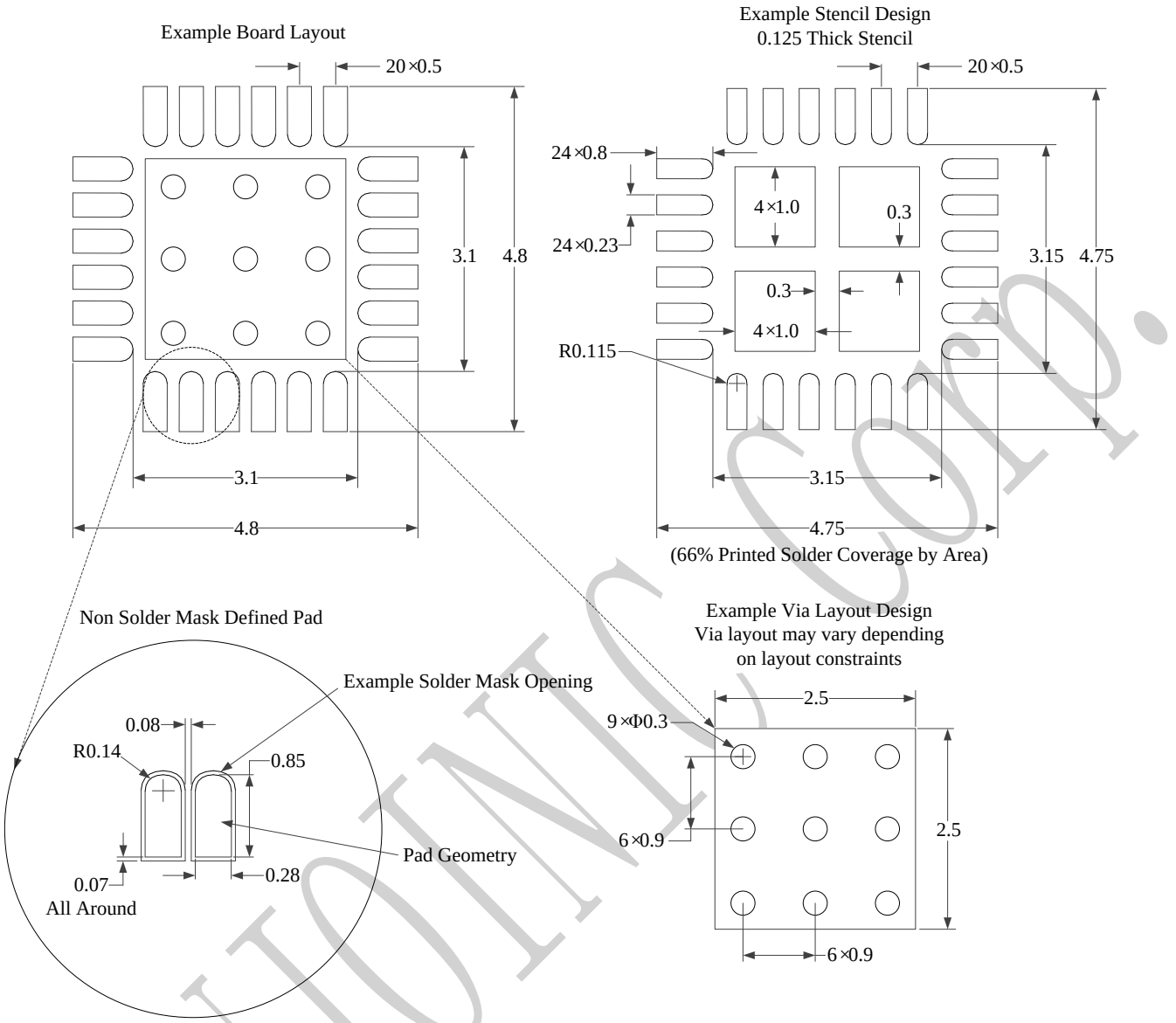
IP2732 realizes OCP overcurrent protection by detecting the current flowing through the sampling resistor. The overcurrent threshold can be flexibly set. When the current reaches the over-current threshold, the over-current abnormal protection occurs, and the Gate will be pulled low, closing the external path NMOS transistor. If the abnormal event disappears, the Type-C handshake and PD communication will be re-established.

12.Package



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.40	2.50	2.60
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.40	2.50	2.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40

13.Layout Design



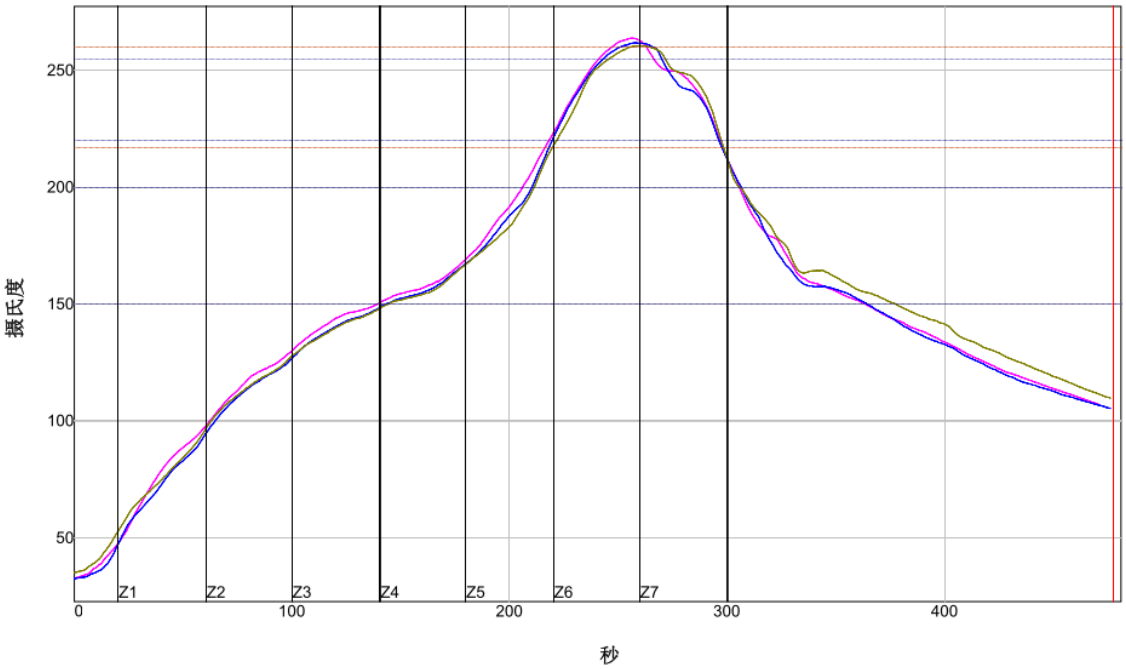
NOTES: 1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

14. Solder Instruction

温度设置 (摄氏度)

温区	1	2	3	4	5	6	7
上温区	130	140	160	160	200	320	265
下温区	130	140	160	160	200	320	265

传送带速度 (公分/分): 39.0



PWI= 75%	最高上升斜率		预热150至200C		最高温度		总共 时间 /217C		斜率1 (217-260C)		预热220至255C-(2)		总共 时间 /260C-2		距峰值5C区域时间	
VP 1	1.69	-31%	66.21	-59%	263.87	18%	80.99	-70%	1.70	-30%	22.81	-36%	15.90	-30%	18.13	-75%
VP 2	1.99	-1%	66.91	-54%	261.84	-9%	78.97	-73%	1.87	-13%	23.44	-33%	15.74	-31%	23.64	-31%
VP 3	1.83	-17%	66.61	-56%	260.76	-23%	78.19	-74%	1.88	-12%	23.97	-30%	9.37	-66%	23.95	-28%
温差	0.30		0.70		3.11		2.80		0.18		1.16		6.53		5.82	

制程界限:

锡膏: 260

统计数名称	最低界限	最高界限	单位
最高温度上升斜率 (目标=2.0) (计算斜率的时间距离= 20 秒)	1.0	3.0	度/秒
斜率1 (目标=2.0) 介于 217.0 和 260.0 (计算斜率的时间距离= 10 秒)	1.0	3.0	度/秒
预热时间150-200摄氏度	60	90	秒
预热时间220-255摄氏度-(2)	10	50	秒
最高温度	255	270	度 摄氏度
在217摄氏度以上时间	60	200	秒
在260摄氏度以上时间-(2)	3	40	秒
距峰值5C区域时间	15	40	秒

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